Gp 2815

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Eugene Lee	
Serial No.:	09/467,992	Group Art Unit: 2815	
Filed:	December 20, 1999	Docket: 303.389US2	
Title:	CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED SEMICONDUCTOR SURFACES		

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on October 29, 2002. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect cancellation of claim 51, amendment of previously pending claims 26, 31, 35, 36, 40, 41, 43-50. The specific amendments to individual claims are detailed in the following marked up set of claims.

26. (Amended) A memory device, comprising:

an array of memory cells, each memory cell including [an] a vertical access transistor that is coupled to a trench capacitor wherein a first plate of the trench capacitor is integral with a second source/drain region so as to form a conductorless electrical connection between the trench capacitor and the vertical access transistor, the first plate including a micro-roughened surface layer of porous polysilicon, and a second plate of the trench capacitor disposed adjacent to the first plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at a first source/drain region of the vertical access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of vertical access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.